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EXAMINER	
GEIB, BENJAMIN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/032,144	ROUSSEL, PATRICE	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-23,93-105 and 107-120* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-23,93-105 and 107-120* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 19, 20, 22, 93, 98, 99, 100, 101 and 109 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sidwell et al., European Patent Application EP 0 743 594 Al, cited on the information disclosure statement filed on June 9,2003 (herein referred to as Sidwell).

3. Referring to claim 19, Sidwell has taught a method comprising:

storing a plurality of non-continuous groups of source bits into a plurality of noncontiguous groups of destination storage locations in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into a plurality of non-contiguous groups of destination storage locations *[Figure 6, page 6, lines 1-14, rep4p, In this instruction the 8 source bits of S[0] are stored at destination R[0], the 8 source bits of S[1] are stored at destination R[1], the 8 source bits of S[2] are stored at destination R[2] and the 8 source bits at S[3] are stored at destination R[3]. So the bits in S[0] and S[3] and non-contiguous groups of source bits that are stored into a plurality of noncontiguous groups of destination storage locations R[0] and R[3].]*; and

duplicating bits from the plurality of non-contiguous groups of storage locations into groups of destination storage locations adjacent to the non-continuous groups of destination storage locations *[Figure 6, page 6, lines 1-14, rep4p, The storage locations R[0] and R[3] are duplicated into storage locations R[4] and R[7]. R[3] and R[4] are adjacent storage locations.]*.

4. Referring to claim 20, Sidwell has taught the method of claim 19, as described above, and in which the source bits are stored in a first register *[Figure 6, element 104]*.

5. Referring to claim 22, Sidwell has taught the method of claim 19, as described above, and in which the source bits are stored in a first memory location *[Figure 6, element 104]*.

6. Referring to claim 93, Sidwell has taught an apparatus comprising:

a first storage area to store a plurality of non-contiguous groups of source bits in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into a plurality of non-contiguous groups of destination storage locations *[Figure 6, page 6, lines 1-14, rep4p, In this instruction the 8 source bits of S[0] are stored at destination R[0], the 8 source bits of S[1] are stored at destination R[1], the 8 source bits of S[2] are stored at destination R[2] and the 8 source bits at S[3] are stored at destination R[3]. So memory R is the first storage area that stores a plurality of non-contiguous groups of source bits, the 8 bits in R[0] and the 8-bits in R[3] .]*; and

a second storage area to store contiguous duplicates of the plurality of noncontiguous groups of source bits *[Figure 6, page 6, lines 1-14, rep4p, The storage locations R[0] and R[3] are duplicated into storage locations R[4] and R[7]. R[3] and R[4] are adjacent storage locations. So memory R is the second storage area that stores contiguous duplicates of the plurality of noncontiguous groups of source bits.]*.

7. Referring to claim 98, Sidwell has taught the apparatus of claim 93, as described above, and wherein the second storage area is to store only two of the plurality of non-contiguous groups of source bits and their duplicates *[Figure 6, page 6, lines 1-14, rep4p, Only two duplicates of each source value is stored.]*.

8. Referring to claim 99, Sidwell has taught the apparatus of claim 93, as described above, and wherein the first and second storage areas are to store data corresponding to multi-media instructions *[Figure 6, page 6, lines 1-14, Data corresponding to the rep4p instruction is stored in the first and second storage areas.]*.

9. Referring to claim 100, Sidwell has taught the apparatus of claim 99, as described above, and further comprising an execution unit to execute the multi-media instructions *[Figure 1]*.

10. Referring to claim 101, Sidwell has taught a system comprising:

a memory to store a plurality of instructions *[Figure 1, page 2, lines 1-38, element 22]*;

a processor to fetch a first instruction from the memory *[Figure 1, page 2, lines 1-38, element 8]*, wherein the first instruction, if executed by the processor, is to cause the processor to store contiguous duplicates of a plurality of non-contiguous groups of source bits into a plurality of groups of destination storage locations without the first instruction specifying an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of groups of destination storage locations *[Figure 6, page 6, lines 1-14, rep4p, In this instruction the 8 source bits of S[0] are stored at destination R[0], the 8 source bits of S[1] are stored at destination R[1], the 8 source bits of S[2] are stored at destination R[2] and the 8 source bits at S[3] are stored at destination R[3]. So the bits in S[0] and S[3] and non-contiguous groups of source bits that are stored into a plurality of noncontiguous groups of destination storage locations R[0] and R[3]. The storage locations R[0] and R[3] are duplicated into storage locations R[4] and R[7]. R[3] and R[4] are adjacent storage locations.]*.

11. Referring to claim 109, Sidwell has taught the system of claim 101, as described above, and wherein the processor is to fetch a second instruction from the memory *[Figure 6, page 6, lines 1-14, rep4p]*, the second instruction to store a first number of non-contiguous duplicates of a second number of contiguous groups of source bits into a destination storage location, the first number being larger than the second number *[The source of S is always 64 bits, or eight 8-bit locations. S[0] and S[3] are stored into R[0] and R[3] as well as R[4] and R[7]. Two (8-bit duplicates) is less than eight (8-bit source locations))).]*.

12. Claims 110-120 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Abdallah et al., US Patent 6,115,8 12 (herein after Abdallah).

13. Referring to claim 110, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:

storing bits (31-0) of a source value into bit storage locations (63-32) and (31-0) of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*,

storing bits (95-64) of the source value into bit storage locations (127-96) and (95-64) of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*.

14. Referring to claim 111, Abdallah has taught the machine-readable medium of claim 110, as described above, and wherein the source value is stored in a memory location *[Figure 3E, column 6, lines 42-55, element 350]*.

15. Referring to claim 112, Abdallah has taught the machine-readable medium of claim 110, as described above, and wherein the source value is stored in a register *[Figure 3E, column 6, lines 42-55, element 350]*.

16. Referring to claim 113, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

storing bits (63-32) of a source value into bit storage locations (31-0) and (63-32) of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*,

storing bits (127-96) of the source value into bit storage locations (127-96) and (95-64) of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*.

17. Referring to claim 114, Abdallah has taught the machine-readable medium of claim 113, as described above, and wherein the source value is stored in a memory location *[Figure 3E, column 6, lines 42-55, element 350]*.

18. Referring to claim 115, Abdallah has taught the machine-readable medium of claim 113, as described above, and wherein the source value is stored in a register *[Figure 3E, column 6, lines 42-55, element 350]*.

19. Referring to claim 116, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

storing only bits (63-32) of a source value into bit storage locations (127-96) and (63-32) of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is CDCD]*,

storing only bits (31-0) of the source value into bit storage locations (31-0) and (95-64) of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is CDCD]*.

20. Referring to claim 117, Abdallah has taught the machine-readable medium of claim 116, as described above, and wherein the source value is stored in a memory location *[Figure 3E, column 6, lines 42-55, element 350]*.

21. Referring to claim 118, Abdallah has taught the machine-readable medium of claim 116, as described above, and wherein the source value is stored in a register *[Figure 3E, column 6, lines 42-55, element 350]*.

22. Referring to claim 119, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:

storing bits [31-0] of a source value into bit storage locations [31-0] of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*;

duplicating bits from the bits storage locations [31-0] to bit storage locations [63-32] of the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*;

Storing bits [95-64] of the source value into bit storage locations [95-64] of the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*; and

Duplicating bits from the bit storage locations [95-64] to bit storage locations [127-96] of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*.

23. Referring to claim 120, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

storing bits [63-32] of a source value into bit storage locations [63-32] of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*;

duplicating bits from the bit storage locations [63-32] to bit storage locations [31-0] of the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*;

storing bits [127-96] of the source value into bit storage locations [127-96] of the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*; and

duplicating bits from the bit storage locations [127-96] to bit storage locations [95-64] of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 21, 23, 94,95,96, 97, 102, 103, 104, 105, 107 and 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sidwell.

26. Referring to claim 21, Sidwell has taught the instruction of claim 19, as described above. Sidwell has not taught the source bits representing a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 138 1, 1385,217 USPQ 401,404 (Fed. Cir. 1983). In re Lowry, 32 F.3d 1579, 32 USPQ2d 103 1

(Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source bits represent any type of data, including double floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above.

27. Referring to claim 23, Sidwell has taught the instruction of claim 19, as described above. Sidwell has not taught the source representing a single-precision floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source represent any type of data, including single-precision floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above.

28. Referring to claim 94, Sidwell has taught the apparatus of claim 93, as described above. Sidwell has not taught the source bits representing a double-precision floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385,2 17 USPQ 401,404 (Fed. Cir. 1983)I In re Lowry, 32 F.3d 1579,32 USPQ2d 103 1 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source bits represent any type of data, including double-precision floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above.

29. Furthermore, Sidwell has not taught that the plurality of non-contiguous groups of source bits is to represent a 32 bit value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the plurality of non-contiguous groups of source bits of Sidwell be any

number of bits, including 32-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459,463, 105 USPQ 237,240 (CCPA 1955).

30. Referring to claim 95, Sidwell has taught the apparatus of claim 94, as described above. Sidwell has not taught wherein the first storage area comprises a 128-bit memory location. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first storage area of Sidwell be any number of bits, including 32-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237,240 (CCPA 1955).

31. Referring to claim 96, Sidwell has taught the apparatus of claim 94, as described above. Sidwell has not taught wherein the first storage and second storage areas comprises a 128-bit memory location. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first storage and second storage areas of Sidwell be any number of bits, including 128-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459,463, 105 USPQ 237,240 (CCPA 1955).

32. Referring to claim 97, Sidwell has taught the apparatus of claim 93, as described above. Sidwell has not taught wherein the plurality of non-contiguous groups of source bits comprise four single-precision floating point values. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention fRom the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385,217 USPQ 401,404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579,32 USPQ2d 103 1 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source represent any type of data, including single-precision floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the plurality of non-contiguous groups of source bits of Sidwell comprise any number of values, including four, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459,463,105 USPQ 237,240 (CCPA 1955).

Referring to claims 102, 103, 104 and 105, Sidwell has taught the system of claim 101, as described above. Sidwell has not taught wherein the plurality of non-contiguous groups of source bits include: a least significant 32 source bits, a most significant 32 source bits, a second most significant group of 32 source bits and a second least-significant group of 32 source bits. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing of data would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 138 1, 1385, 217 USPQ 401,404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 103 1 (Fed. Cir. 1994).

33. Referring to claims 107 and 108, Sidwell has taught the systems of claims 104 and 105, as described above. Sidwell has not taught wherein the first instruction is a MOVSHDUP or a MOVSLDUP instruction. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the name of the instruction. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381,1385,217 USPQ 401,404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 103 1 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions be labeled anything, including, MOVSHDUP and MOVSLDUP, because merely labeling the instructions differently from that in the prior art would have been obvious. See Gulack cited above.

Response to Arguments

34. Applicant's arguments filed 10/23/2008 have been fully considered but they are not persuasive.

35. Applicant argues the novelty/rejection of the claims, in substance, that:

> a) "Sidwell fails to disclose at least 'storing a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to execution of a first instruction' and 'duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations' as required by claim 19." (1st paragraph on page 10);

b) "Abdallah fails to disclose at least 'wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register' as required by claim 110." (last paragraph on page 12)

36. These arguments are not found persuasive for the following reasons:

Regarding point a, specifically the applicant's assertion that Sidwell fails to disclose "storing a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to execution of a first instruction," the examine notes that the applicant appears to be reading the claims too narrowly. The applicant argues that because S[0], S[1], S[2], and S[3] are contiguous groups of source bits that therefore Sidwell fails to disclose "storing a plurality of non-contiguous groups of source bits . . . ." However, this is incorrect. Although S[0], S[1], S[2], and S[3] are, as noted by the applicant, contiguous groups of source bits, the claim does not require that contiguous groups of source bits are not stored. Instead, the claim merely requires that a plurality of non-contiguous groups of source bits are stored. Sidwell has taught storing both contiguous and non-contiguous groups of source bits depending upon what groups of source bits are considered [Figure 6, page 6, lines 1-14, rep4p]. If the applicant intends for the claims to be read as storing only non-contiguous groups of source bits, then the claims should be amended to require such a reading.

Further regarding point a, specifically the applicant's assertion that Sidwell fails to disclose "duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations," the examiner notes that the claims language does not require that all groups of storage locations be adjacent to the non-contiguous groups of destination storage locations, but merely that one of the groups be adjacent to them. As described in the rejection of claim 19 and noted by the applicant in the remarks, R[3] and R[4] are adjacent. Therefore, Sidwell has taught "duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations" as claimed.

Regarding point b, the applicant argues that because Abdallah has not explicitly mentioned how the order of the source bits stored in the destination are specified that Abdallah has therefore not taught that the "instruction does not include a code to designate the order in which the source bits are to be

stored in the destination register." This is incorrect. Simply because Abdallah is silent on the order designation does not require that the instruction must include a code to designate the order. The examiner notes that the above-cited claim language is describing the invention in terms of what it is not, rather than what it is. In such an instance, as long as Abdallah does not contradict the claim language Abdallah has taught the invention as claimed. Therefore, Abdallah has taught "wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register" as recited in claims 110, 113, 116, 119, and 120. Regarding the applicant's as to why result 354 (in claim 110) is "BBDD" but not otherwise, the examiner notes that Abdallah has taught that the result may be any one of the result organizations possible by shuffling the four source elements [column 6, lines 42-55]. Abdallah states that "In the illustrative example of FIG. 3E, any of the four data elements A, B, C, and D of the operand 350 can be stored in any of the locations of the result 354." [column 6, lines 50-53] Therefore, "BBDD" (as well as the other results indicated in claims 113, 116, 119, and 120) is a result contemplated by Abdallah and the statement of that result merely indicates that when the result is such the recited claim language is met.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib
Examiner
Art Unit 2181

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/Niketa I. Patel/

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